Improving the cache performance of multicore processors

# Abstract

Cache is defined as the memory that is positioned logically between registers and main memory with capacity less than main memory and greater than registers. Cache memory is used mainly to improve the system performance by reducing the time needed to access memory.

As the demand for technologies like multithreading, multimedia, database and low power devices that run on high performance multicore processors using higher associativity to enrich performance is increasing, even the need for designing highly efficient cache memory is also increasing. In present situation the trend is multicore architectures and this concept is ruling the recent microprocessor design mainly because of the following reasons: better performance, ease/reuse of design, thread level parallelism, better thermal and power scaling.

There is growing need for efficient cache memory utilization in Multicore architectures and also Modern Database System because the significant amount of execution time is spent on second level (L2) data cache misses and first level (L1) instruction cache misses.

Main aim of this project is to improve the cache performance of multicore processors. Our goal is to identify the cache performance issues of multicore processors and address the same with various optimization methods and implement the same. Benefits of improving cache performance in multicore processors will be reduced number of instruction cache misses, increased temporal and spatial instruction locality, less overhead and decreased number of branch mispredictions.

Keywords: Cache performance of multi-core processors, Cache optimization, spatial locality, Cache-hit, Cache-miss, Penalty, Cache size.

Languages used: Data Structures, C and OpenMP

Members:

* SNEHA.D.L (12MCS1037)
* P.L.PADMASREE (12MCS1012)